IN THE DRAWINGS

The drawings as filed on May 10, 2002 are accepted by the Examiner. However, in the instant Office Action, the Examiner requested that Applicants resubmit pages 1-2 of the drawings as a working set of the drawings with the Examiner's notes (instead of the file copy) was inadvertently scanned.

Applicants hereby resubmit pages 1-2 of the drawings.

REMARKS

Applicants acknowledge that, in view of the Amended Appeal Brief filed on December 14, 2005, the Examiner has reopened prosecution of the pending application and new grounds of rejection have been presented. Claims 1-24 remain pending in this application.

In the pending Office Action dated March 10, 2006, the Examiner objected to claims 2, 4, 5, 9, 11, 14, 15, 17, 18, 19, 20, and 23 due to informalities. In light of the amendments and arguments presented herein, Applicants believe that the Examiner's objections and concerns have been addressed.

Examiner's request for the drawings and the Abstract have been addressed. Clean copies of the Abstract and the drawings are attached herewith.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Applicants respectfully traverse this rejection.

Regarding claims 1, 4, 18, and 21 Applicants respectfully assert that the term "said plurality of ESD clamp devices being connected to a corresponding one of said plurality of turns of said inductor" is not indefinite because it would be known to those skilled in the art having benefit of the present disclosure that this term refers to each ESD clamp being connected to one of the turns the inductor in a corresponding or separate manner. Therefore, claims 1 and 4 are not indefinite and accordingly, Applicants respectfully request the Examiner withdraw the rejection of claims 1, 4, 18, and 21 under 35 U.S.C. 112, second paragraph.

Regarding claims 6 and 7, Applicants respectfully assert those skilled in the art having benefit of the present disclosure would know that the term "each of the plurality of conductive

vias is at least one via" is not indefinite since it could be construed to mean that the plurality of conductive vias may be actually one single via (claim 6) of two separate vias (claim 7).

Claim 11 has been amended to depend from claim 4, and therefore, the antecedent basis for the term "plurality of conductive layers" is present and the rejection of claim 11 is now moot. In light of the amendments and arguments presented herein, claims 1-24 are allowable.

The Examiner rejected claims 1-3 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,969,929 (***Kleveland***). Applicants respectfully traverse this rejection.

Kleveland does not teach, disclose, or make obvious all of the elements of claims 1-3 of the present invention. In the Office Action dated March 10, 2006, the Examiner operates on the false assumption that ***Kleveland*** discloses the invention expect for the element of the plurality of ESD clamp devices being connected to an inductor. The Examiner claims that since it was allegedly known that at the time of the invention, the use of additional clamp devices to provide additional ESD protection would have been obvious. Firstly, it is false that ***Kleveland*** discloses all elements of the invention except for a plurality of ESD clamp devices being connected to an inductor. ***Kleveland*** does not several elements of the present invention. Secondly, the Examiner provides no evidence or arguments to support the conclusory statement that allegedly, the plurality of EDS clamp devices would be obvious. It is insufficient to merely state, without evidence that it would have been obvious to connect a plurality of ESD devices to an inductor when the prior art does not disclose that subject matter. Further, ***Kleveland*** is missing more than the element of the plurality of ESD clamps, as described in further details below.

In fact, ***Kleveland*** actually teaches away from the low pass filter called for by claims of the present invention. In the Office Action dated March 10, 2006, the Examiner fails to cite a low pass filter structure in ***Kleveland*** and resorts to an external definition of a low pass filter in the Illustrated Dictionary of Electronics. This is tantamount to ignoring what is disclosed in ***Kleveland*** or in the specification of the present invention and going directly to a third source to support the Examiner's arguments. ***Kleveland*** affirmatively disavows low pass filter as described below. Therefore, ***Kleveland*** teaches away from the invention called for by claims 1-3 of the present invention.

The Examiner misconstrued the disclosure in the Specification, relating to the discussion of reducing the shunt capacitance of the ESD clamp device and equated it to ***Kleveland's*** disclosure of promoting a reduction in the parasitic capacitance. However, the Examiner missed the point in the Specification, which discloses that a reduction in the shunt capacitance of the ESD clamp device is present "...for signal frequencies below the low pass filter cutoff frequency." (emphasis added). *See*, Specification, page 4, lines 3-5. Apparently, the Examiner missed the point that any reduction in the shunt capacitance of the ESD clamp is for low frequency signals (frequencies below the low pass filter cut-off frequency). Basically, this passage provides for a low pass filter. This is in direct contradiction to ***Kleveland's*** disclosure, which allows high frequency signals to pass (*i.e.*, a high pass filter). Therefore, ***Kleveland*** discloses the opposite of a low pass filter. Hence, ***Kleveland*** clearly does not anticipate all of the elements of claims 1-3 of the present invention.

Kleveland affirmatively asserts that the circuitry disclosed is not a low pass filter, but calls for high performance required by high frequency applications. *See* col. 5, lines 22-26.

Kleveland clearly asserts that at low frequencies, the circuit is protected from ESD discharge events, at the same time, the ESD protection circuit provides high performance required by high frequency applications. Further, ***Kleveland*** expressly asserts that for high frequency signals, its ESD circuit performs like a transmission line. *See* col. 5, lines 21-22. Therefore, ***Kleveland*** expressly discloses that its system is not a low pass filter.

In contrast to ***Kleveland***, claim 1 in the present invention calls for forming a low pass filter. ***Kleveland*** indeed teaches the opposite subject matter as compared to the elements called for by claim 1 of the present invention. ***Kleveland*** is directed towards reducing capacitance of ESD protection and promoting a reduction of the parasitic capacitance in an attempt to avoid reducing the bandwidth of high frequency devices. In contrast to disclosure in ***Kleveland***, claim 1 calls for the ESD devices being connected to a plurality of turns of an inductor, where the inductor and the parasitic capacitance of the ESD device are used to form a low pass filter. In other words, for high frequency signals, the parasitic capacitance of the ESD device of the present invention is useful in performing a low pass filtering process. Therefore, ***Kleveland*** performs the opposite of the claimed elements. Upon an examination of ***Kleveland***, those skilled in the art would be directed away from the claims of the present invention. ***Kleveland*** discloses attempting to reduce or eliminate parasitic capacitance, wherein claims of the present invention call for using the inductance of the turns, in combination with the parasitic capacitance to form a low pass filter. Therefore, ***Kleveland*** does not disclose all of the elements of the claimed invention. In addition, ***Kleveland*** actually teaches away from the claims of the present invention.

It is perfectly clear that the disclosure of ***Kleveland*** does not seek to prevent high frequency transmissions; in fact, it clearly states that the ESD protection 240 of ***Kleveland***

performs like a transmission line during high frequency transmission. This is opposite of what is called for by claims 1-3 of the present invention, which call for a low pass filter, thereby substantially restricting high frequency signals. Therefore, Examiner's assertion that ***Kleveland*** allegedly provides identical structure except for the plurality of ESD clamp devices being connected to an inductor, is unfounded and not supported by the disclosure of ***Kleveland***. In fact, the disclosure of ***Kleveland*** clearly supports the opposite assertion and ***Kleveland*** does not disclose elements called for by claim 1 of the present invention, including the element of forming the low pass filter. Therefore, ***Kleveland*** does not anticipate all of the elements of the claims of the present invention. Additionally, Applicants respectfully assert that ***Ling*** does not add disclosure to make up for the missing elements of claims 1-3 that is not taught by ***Kleveland***. In fact, since ***Kleveland*** teaches away from the elements of the claims of the present invention, simply combining ***Ling*** would not make obvious all of the elements of the present invention. These arguments are discussed in more details below. Therefore, claims 1-3 of the present invention are not taught, disclosed, or suggested by the cited prior art and, thereby, are allowable.

As described above, ***Kleveland*** does not teach, disclose, or suggest all of the elements of claims 1-3 of the present invention. ***Kleveland*** actually directs one away from the present invention. ***Kleveland*** is directed towards reducing parasitic capacitance of ESD protection circuits. *See* col. 1, lines 35-38. ***Kleveland*** promotes reducing parasitic capacitance in an attempt to avoid reducing the bandwidth of high frequency devices. *See* col. 2, lines 5-8. ***Kleveland*** is directed to attempt reducing or eliminating the parasitic capacitance to reduce data transmission errors. In contrast to ***Kleveland***, claims 1-3 of the present invention call for a plurality of ESD clamp devices being connected to a corresponding one of a plurality of turns on an inductor, wherein the inductor and the parasitic capacitance is used to form a low pass filter.

Additionally, ***Kleveland*** does not mention the utilization of parasitic capacitance. ***Kleveland*** merely mentions the undesirability of parasitic capacitance, wherein claims of the present invention utilize turns of an inductor in conjunction with the parasitic capacitance of the ESD clamp devices to form a low pass filter. Therefore, ***Kleveland*** does not teach or make obvious all of the elements of claims 1-3.

Furthermore, claims 1-3 also call for an inductor coil for generating an inductance for the low pass filter. As admitted by the Examiner in the Office Action dated March 10, 2006, the disclosure in ***Kleveland*** does not disclose the plurality of ESD clamp devices with the parasitic capacitance being connected to corresponding turns of an inductor to form a low pass filter. In fact, ***Kleveland*** directs one away from the parasitic capacitance and, therefore, does not disclose the low-pass filter elements called for by claim 1 of the present invention. The mere conculsory statement by the Examiner that it would have been obvious to connect the ESD devices to an inductor is not supported arguments or evidence. Further, the elements of claims 1-3 actually calls for more that just a plurality of ESD devices being connected to an inductor. The claims also calls for plurality of ESD clamp devices with the parasitic capacitance being connected to corresponding turns of an inductor to form a low pass filter, which as described herein is not taught or made obvious by ***Kleveland***. Other cited prior art does not make up for this deficit. Therefore, claims 1-3 of the present invention are allowable. Accordingly, claims 1-3 are allowable.

Independent claim 1 is allowable for at least the reasons cited above. Additionally, dependent claims 2-3, which depend from independent claim 1, are also allowable for at least the reasons cited above.

The Examiner rejected claims 4-24 under 35 U.S.C. 103(a) as being unpatentable over ***Kleveland*** in view of U.S. Patent 5,576,680 ***(Ling)***. Applicants respectfully traverse this rejection.

Applicants respectfully assert that contrary to Examiner's statements in the Office Action dated March 10, 2006, a prima facie case of obviousness has not been established to uphold the rejection of claims 4-24. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to the alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or

modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success viewed in light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Applicants respectfully assert that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art references (***Kleveland*** and ***Ling***) do not teach or make obvious all of the claim limitations of the claims of the present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***Kleveland*** and ***Ling***). In fact, Applicants provide arguments that ***Kleveland*** and ***Ling*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claims 4-24 of the present invention.

The Examiner asserted that all elements of claims 4-13, 15-18, and 20-24 are allegedly disclosed by ***Kleveland*** except for the element of each of the turn of one inductor being formed on a separate layer of the integrated circuit. Applicant respectfully assert that ***Kleveland*** does not disclose many of the elements of claims 4-13, 15-18, and 20-24 and ***Ling*** does not make up for this deficit. As described above, the Examiner's assertion that ***Kleveland*** allegedly provides

identical structure except for the plurality of ESD clamp devices being connected to an inductor, is unfounded and not supported by the disclosure of ***Kleveland***. In fact, the disclosure of ***Kleveland*** clearly supports the opposite assertion and ***Kleveland*** does not disclose elements called for by claim 4-13, 15-18, and 20-24 of the present invention, including the element of forming the low pass filter. Therefore, ***Kleveland*** does not anticipate all of the elements of the claims of the present invention. Further, Applicants respectfully assert that ***Ling*** does not add disclosure to make up for the missing elements of claims 4-13, 15-18, and 20-24 that are not taught by ***Kleveland***. In fact, since ***Kleveland*** teaches away from the elements of the claims of the present invention, simply combining ***Ling*** would not make obvious all of the elements of the present invention. These arguments are discussed in more details below. Therefore, claims 4-13, 15-18, and 20-24 of the present invention are not taught, disclosed, or suggested by the cited prior art and, thereby, are allowable.

Claims 4-13, 15-18, and 20-24 are generally directed to a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter. Claims 4-13, 15-18, and 20-24 are also directed to a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter. In contrast, ***Kleveland*** is directed to reducing capacitance of ESD protection and providing a reduction in the parasitic capacitance in order to maintain the bandwidth of high frequency devices. Therefore, the disclosure of ***Kleveland*** provides for passing high frequency signals, which is in stark contrast with claims 4-13, 15-18, and 20-24. Additionally, the disclosure of ***Ling*** does not compensate for the deficit of ***Kleveland***. For example, ***Ling*** does not disclose ESD protection or utilization of parasitic capacitance with inductor turns to make up for the deficit of ***Kleveland***. ***Ling*** is directed to forming an inductive circuit on a semiconductor chip,

however, ***Ling*** does not disclose the subject matter that is lacking in ***Kleveland,*** but called for by claims of the present invention.

Contrary to the Examiner's assertions, Applicants respectfully assert that ***Ling*** does not disclose that a via could be used to connect coil shaped elements to produce an inductive element, as called for by claim 4 of the present invention. ***Ling*** discloses a via to connect an inductive core to conductive lines, not connecting coil turns on different layers. *See*, col. 4, lines 39-49. Therefore, ***Ling*** does not provide the subject matter that the Examiner uses to combine with ***Kleveland*** in order to make obvious independent claims 4 and 18.

Kleveland does not disclose that each of the turns of the inductor are formed from a separate layer of the integrated circuit. The Examiner seems to use ***Ling*** to provide the inductive circuit 400 by connecting a plurality of inductor coils having a plurality of turns formed from different horizontal planes of the IC chip. *See* col. 7, lines 59-col. 8, line 7. However, Applicants respectfully assert that the addition of ***Ling*** does not make up for the deficits of ***Kleveland***. One reason is because ***Kleveland*** does not disclose the use of the parasitic capacitances provided by the plurality of ESD clamp devices being coupled to corresponding turns of an inductor to form a low pass filter. ***Ling*** does not provide this disclosure; therefore, the mere addition of ***Ling*** does not make up for the deficit of ***Kleveland***. Also, ***Ling*** does not disclose the element that the Examiner claims is missing from ***Kleveland***, e.g., a via used to connect coil shaped inductive elements to produce an inductive element, as called for by in claim 4 of the present invention.

Further, ***Ling*** simply does not disclose ESD protection or utilization of parasitic capacitance with inductor turns to make up for the deficit of ***Kleveland***. ***Ling*** is merely directed

to forming an inductive circuit on a semiconductor chip. ***Ling*** provides for patterned lines to form an inductor. Although ***Ling*** discloses a plurality of inductor elements formed on different horizontal planes, ***Ling*** does not disclose the subject matter that is lacking in ***Kleveland,*** but called for by claims of the present invention. *See* col. 7, lines 59-65. Therefore, combining ***Kleveland*** and ***Ling*** would still not disclose the elements of utilizing a plurality of ESD clamp devices with a parasitic capacitance being connected to corresponding turns of an inductor in order to provide a low pass filter, as called for by claim 4 of the present invention. Therefore, claims 3-17, which directly or indirectly depend from claim 4, are not taught, disclosed, or made obvious by ***Kleveland***, ***Ling***, or their combination. Further claim 14, which depends from claim 4, is also allowable for the reasons cited herein. Additionally, claim 18, which provides a method for forming a plurality of conductive layers provides ESD clamp devices, which are then connected to corresponding coil turns to form a low pass filter for at least the reasons described above. Therefore, claim 18 of the present invention is allowable. Additionally, claims 19 and 20, which depend from claim 18 are also allowable for similar reasons cited above. Furthermore, previously added claim 21, which calls for a device comprising a plurality of ESD clamp devices with a parasitic capacitance being connected to corresponding turns of an inductor, in order to provide a low pass filter, is also not taught or made obvious by ***Kleveland***, ***Ling***, or their combination, for at least the reasons cited above.

As described above, ***Kleveland***, ***Ling***, or their combination, do not disclose or make obvious a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter, which are elements of claim 4, from which claim 10 indirectly depends. ***Kleveland***, ***Ling***, or their

combination, also do not disclose a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter, which are elements of claim 4, from which claim 10 indirectly depends. Therefore, claim 10 is not anticipated or made obvious by ***Kleveland***, ***Ling***, or their combination.

Additionally, claim 10 also calls for the conductive layer being made from metal, which is selected from the group consisting of copper, aluminum, copper alloy and aluminum alloy. There is no disclosure in ***Kleveland***, ***Ling***, or their combination that provides for the novel formation of conductive layers, as well as the conductive layers being made from a metal, which is selected from a group consisting of copper, aluminum, copper alloy and aluminum alloy. ***Kleveland***, ***Ling***, or their combination do not anticipate or make obvious such subject matter. Therefore, claim 10 is allowable for at least the reasons cited herein.

As described above, ***Kleveland***, ***Ling***, or their combination, do not disclose or make obvious a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter, which are elements of claim 4, from which claims 12 and 13 depend. ***Kleveland***, ***Ling***, or their combination also do not disclose a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter, which are elements of claim 4, from which claims 12 and 13 depends. Therefore, claims 12 and 13 are not anticipated or made obvious by ***Kleveland***, ***Ling***, or their combination.

Additionally, claim 12 calls for a magnetic material that is provided concentrically inside of an inner diameter of the coil turns of the plurality of conductive layers. This provides for an

increase of the inductance thereof. The use of the concentrically positioned magnetic material to increase the inductance is not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. No subject matter to this effect is provided neither in ***Kleveland*** nor in ***Ling***. Therefore, all of the elements of claim 12 are not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. Accordingly, claim 12 is allowable for at least the reasons cited herein.

Furthermore, claim 13, which depends from claim 12, provides the additional element of the magnetic material being of a material that is selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide. As described above, ***Kleveland***, ***Ling***, or their combination do not disclose or make obvious the magnetic material called for by claim 13. Additionally, ***Kleveland***, ***Ling***, or their combination also do not disclose the use of the material selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide for the magnetic material. Therefore, all of the elements of claim 13 are not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. Accordingly, claim 13 is allowable for at least the reasons cited herein. For at least the reasons cited above, claims 12 and 13 of the present invention are also allowable.

Furthermore, contrary to the Examiner's assertions in the Office Action dated March 10, 2006, Applicants respectfully assert that one skilled in the art would not combine ***Kleveland*** and ***Ling*** to make obvious all of the claims of the present invention. ***Kleveland*** is directed to distributed ESD protection in a device, wherein ***Ling*** is directed to forming an inductor on a substrate using line patterns and an inductive core. Without improper hindsight, one skilled in the art would not combine the teaching of ***Kleveland*** and ***Ling*** to make obvious all of the claims of the present invention. Contrary to the Examiner's position, Applicants assert that, without

gleaning only from Applicants' disclosure, a reconstruction of elements of the claimed invention would not be possible. There is no indication in either prior art (***Kleveland*** or ***Ling***) that a via could be used to connect coil shaped elements to produce an inductive element, as described in the Specification and claimed in claim 4 of the present invention. *See* pages 10-11 of the Specification. ***Ling*** discloses a via to connect an inductive core to conductive lines, not connecting inductive coils on different layers. *See*, col. 4, lines 39-49 of ***Ling***. Therefore, one skilled in the art would not be motivated to combine ***Ling*** with ***Kleveland*** to make obvious all of the elements of the present invention. Hence, one would need improper hindsight by gleaning only from Applicants' disclosure to make obvious all of the elements of the claims of the present invention. However, *arguendo*, even if ***Kleveland*** and ***Ling*** were combined, all of the elements of the claims of the present invention would not be obvious to those skilled in the art as described above. Additionally, claims 4-24 are also not made obvious by ***Kleveland***, ***Ling*** or their combination for at least the reasons described above. Accordingly, Applicants respectfully assert that the rejection of claims 4-24 under 35 U.S.C. § 103(a) is erroneous because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Kleveland***, ***Ling***, or their combination. Therefore, claims 4-24 are allowable. Further claims

Reconsideration of the present application is respectfully requested.

In light of the arguments presented above, Applicants respectfully assert that claims 1-24 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is respectfully requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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